REMARKS

Examiner Hung S. Bui is thanked for thoroughly reviewing the instant application and for examining the Prior Art.

Examiner is also thanked for the indication of allowing claims 6-17, 25,34, 40-51 and 59-68 if these claims are rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Favorable reconsideration of this application in light of the above amendments and the following remarks is respectfully requested.

A new method is provided for mounting a semiconductor on the surface of a Printed Circuit Board. A layer of Elastomer is deposited on the surface of the PCB, this layer of Elastomer makes the PCB into a thermally compliant PCB such that the thermal mismatch between the PCB and the semiconductor die that is mounted on the PCB is sharply reduced. Openings are created in the layer of Elastomer and electrical interfaces are created such that the PCB can be connected to the semiconductor die that is mounted on the PCB.

Claim rejections - 35 U.S.C. § 103(a)

Reconsideration of the rejection of claims 1-5, 18-24, 35-39, 52-58 and 69-72 under 35 U.S.C 103(a) as being unpatentable over Yasue et al. (US Patent 6,217,988) in view of Anderson (US Patent 5,969,461) is respectfully requested based on the following arguments.

Neither Yasue et al. nor Anderson provide for the layer of stress relieve material that is, claim 1 of the instant invention, created over the surface of a circuit board. This layer of stress relieve material is basic and essential to the instant invention and has been extensively highlighted and explained in the specification in addition to being shown in the drawings of the application, for instance layer 48 in Figs. 3, layers 50-52 in Figs. 4a, 4b and layer 48 in Figs. 5a-5c.

Yasue et al. provide for the creation of a multilayer printed circuit board without thereby however providing for, as the essential objectives of the instant invention:

- elimination of thermal stress between a mounted semiconductor die and an underlying Printed Circuit Board

- providing a cost effective method to eliminate thermal stress between a mounted semiconductor die and the underlying Printed Circuit Board, and
- providing a method that allows for direct die attachment to a surface of a Printed Circuit Board without incurring negative results of thermal mismatch between the semiconductor die and the Printed Circuit Board.

Since considerations of stress relieve, more so in the era of ever increasing device packaging densities, are major concerns in the creation of high-density, high-performance semiconductor packages, the advantages that are provided by the invention, as specified in detail by the "one or more layers of thermal stress relieve materials on the surface of said circuit board" of claim 1 and further specified in dependent claims to claim 1, is a significant contribution to the art of packaging semiconductor devices.

Yasue et al. and Anderson provide methods of either providing a semiconductor supporting surface (Yasue et al.) or of mounting a semiconductor device over the surface of a substrate (Anderson), both without further addressing concerns of thermal stress relieve.

Yasue provides detail relating to the creation of the various overlying layers that are comprised in the substrate, such as a resin insulating layer, preferably comprising thermoplastic resin, an adhesive layer preferably formed by dispersing cured particles of a heat-resistant resin, and the like. In all of the specifications that are provided by Yasue et al. these specifications relate to the creation of layers of material that collectively form a multilayer PCB. For none of the layers that are used by Yasue et al. is such a layer deposited over the surface of a circuit board and therefore for none of the layers that are provided by Yasue et al. do these layers address the important aspects of thermal stress relieve, an aspect that is provided for by the instant invention and that in addition is provided in such a manner that the stress relieve layer is not limited to one layer but can for instance be applied in more than one layer, in this manner equally providing for semiconductor packages comprising multiple semiconductor devices that need an extreme amount of stress relieve due to the high degree of heat generated by these multiple semiconductor devices.

Anderson et al. provide for a semiconductor package that is specifically aimed at packaging an acoustic wave device. While this package might be readily adopted to package semiconductor

devices other than acoustic wave devices by providing more points of electrical contact over the surface of the substrate of the package of Anderson, the method that is provided by Anderson also does not address problems of thermal stress relieve, which is the essential aspect of semiconductor packaging that is addressed by the invention. Anderson therefore also makes no provision for providing extended thermal stress relieve capabilities by not providing or referring to creating thermal stress relieve that is not limited to one layer but can be applied in more than one layer, in this manner equally providing for semiconductor packages comprising multiple semiconductor devices that need an extreme amount of stress relieve due to the high degree of heat generated by these multiple semiconductor devices.

Regarding claim 35, Yasue et al. specifically does not address or provide for the essential aspect of the instant invention, that is (claims 1 and 35 of the instant invention): "one or more layers of thermal stress relieve material created on the surface of said circuit board". Yasue et al. therefore also does not provide for, in combination with the thermal stress relieve layers, the mounting of one or more semiconductor devices and the establishment of electrical contact between these semiconductor devices and the underlying circuit board.

The same comments as provided supra relating to Anderson apply to claim 35: Anderson does not address thermal stress relieve, the key aspect of the instant invention that is even further specified by, claims 4 and others, specifying that the layer of thermal stress relieve material preferably comprises elastomer or any other thermal compliant material.

Claim 36 is a dependent claim to claim 35, which as has been argued above is significantly at variance with the methods and packages that have been provided by either Anderson or Yasue et al.

Claim 38 further specifies the material that can be used for the thermal stress relieve layer. Neither Anderson nor Yasue et al. provide for such a layer that is deposited over the surface of a circuit board, even though Yasue et al. discloses a layer of thermally compliant resin material that is part of the PCB that is provided by Yasue et al. The layer of thermally compliant resin provided by Yasue et al. assures that the internal structure of the PCB is thermally compliant without thereby however providing for the thermal adaptation of a circuit board to one or more high-density semiconductor devices that are mounted over the surface thereof. The latter thermal adaptation is provided by the instant invention by one or more

layers of thermal stress relieve material that is, in a cost-effective manner, deposited over the surface of a circuit board, in this manner considerably extending thermal stress handling capabilities of existing circuit boards.

Claim 39 of the instant invention further specifies that methods of PCB technology or methods of Build Up Board can be used concurrent with the application of the one or more thermal stress relieve layers.

Regarding claim 52, the surface roughening that is provided by Yasue et al. is provided for purposes of enhancing adhesion between overlying layers that are internal to a PCB, thus creating a PCB of improved reliability without thereby however addressing aspects of creating a thermal stress relieve layer in a manner that is not detrimental to reliability aspects of the created package. The thermal stress relieve layer, applied in one or more layers, must be applied cost-effectively and reliably. Yasue et al. does not provide a thermal stress relieve layer and therefore does not address aspects of reliability that may arise as a consequence of applying one or more thermal stress relieve layers.

Regarding claim 53, layers of resin are conventionally cured after creation thereof, this however still leaves the Yasue et al. invention without, as argued above, the use of or provision for thermal stress relieve. Once the thermal stress relieve layer or layers have been provided, as provided by the instant invention and at variance with both Yasue et al. and Anderson, the created layer of thermal stress material is further improved if this layer is cured. Since the instance invention must be completely specified, thereby including an optimum use and application of the provisions of the instant invention, the curing of the applied layer of thermal stress relieve material must be specified.

Regarding claims 54-56, since Yasue et al. at no time address or allude to or provide for a thermal stress relieve layer, Yasue et al. will not specify any of the aspects that relate to a provided layer of thermal stress relieve material. Since the instant invention does provide as one of its main aspects for a thermal stress relieve layer, it is incumbent on the instant invention to also specify the options that are available for the best creation of the provided layer of stress relieve material.

Regarding claim 57, Yasue et al. does address contact pads, since without contact pads a semiconductor device could not be made operational. Yasue et al. however does not specify thermal stress release, which is part of the independent claim 35 to which claim 57 is a dependent claim.

Regarding claim 58, comments similar to the comments made above relating to claim 57 apply in this case of claim 58, whereby claim 58 however more specifically addresses how to adapt the provided thermal stress release layer to the environment of creating a completed semiconductor package.

Regarding claims 71 and 72, Examiner notes that Yasue et al. do not disclose the specific application of the instant invention of the process of applying a thermal stress relieve layer as further detailed in claims 71 and 72. It has been argued above that the not providing for a thermal stress layer by Yasue et al. or by Anderson significantly differentiates between the instant invention and the inventions of Yasue et al. and Anderson.

In light of the foregoing response, applicant respectfully requests that the Examiner's rejection of claims 1-5, 18-24, 35-39, 52-58 and 69-72 under 35 U.S.C 103(a) as being unpatentable

over Yasue et al. (US Patent 6,217,988) in view of Anderson (US Patent 5,969,461), be withdrawn.

The prior art made of record and not relied upon that is considered pertinent to Applicant's disclosure, that is Farnworth (US Patent 6,211,052), Wang et al. (US Patent 5,519,177) and Asai et al. (US Patent 5,741,575) have been examined and have been found to be of general interest to the invention. These prior art records however do not teach the extent and the detail combined with the flexibility of the present patent application.

Other Considerations

No new independent or dependent claims have been written as a result of this office action, no new charges are therefore incurred due to this office action.

SUMMARY

A new method is provided for mounting a semiconductor on the surface of a Printed Circuit Board. A layer of Elastomer is deposited on the surface of the PCB, this layer of Elastomer makes the PCB into a thermally compliant PCB such that the thermal mismatch between the PCB and the semiconductor die that

is mounted on the PCB is sharply reduced. Openings are created in the layer of Elastomer and electrical interfaces are created such that the PCB can be connected to the semiconductor die that is mounted on the PCB.

It is requested that should Examiner not find the claims to be allowable that he call the undersigned Attorney at his convenience at 845-452-5863 to overcome any problems preventing allowance.

Respectfully submitted,

George O. Saile

George O. Saile (Reg. No 19,572)